Notice of Allowability	Application No.	Applicant(s)	
	10/689,060	FUKUDA ET AL.	
	Examiner	Art Unit	
	Thinh T. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/21/2003*.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☒ The drawings filed on *21 October 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

DETAILED ACTION

Specification

1. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Reason for allowance

2. Claims 1-18 are allowed.

The following is an examiner's statement of reason for allowance:

I/ Group I: Claims 1-3,10-12:

None of the references of record teaches or suggests the claimed **SEMICONDUCTOR EQUIPMENT** having the limitations:

-- " a plurality of transistors having a source cell and a drain cell disposed alternately on the substrate so as to form a mesh pattern; and upper and lower layer wirings for electrically connecting the source cells and the drain cells,"--

and

-- " the upper layer wiring includes a second source wiring having a plurality of

stripes for connecting to the first source wiring and a second drain wiring having a plurality of stripes for connecting to the first drain wiring, wherein the second source wiring has a width of the stripe, which is wider than that of the first source wiring, and the second drain wiring has a width of the stripe, which is wider than that of the first drain wiring, "--

and all other limitations as recited in claim 1.

II/ Group II: Claims 4-6:

None of the references of record teaches or suggests the claimed **SEMICONDUCTOR EQUIPMENT** having the limitations:

-- "a plurality of lateral type metal oxide semiconductor transistors having a source cell and a drain cell, which are disposed alternately on a principal plane of the substrate so as to form a mesh pattern; and upper and lower layer wirings disposed on the substrate for electrically connecting the source cells and the drain cells, wherein the lower layer wiring includes a first drain wiring for connecting the neighboring two drain cells disposed in a diagonal direction of the mesh pattern, and a first source wiring for connecting the source cells and surrounding the first drain wiring, wherein the upper layer wiring includes a second source wiring disposed perpendicularly to the first source wiring and having a plurality of stripes for connecting to the first source wiring through a source via-hole, and a second drain wiring disposed perpendicularly to the first drain wiring and having a plurality of stripes for connecting to the first drain wiring through a drain via-hole, wherein the second source wiring has a width of the stripe, which is wider than a minimum width of the stripe of the first source wiring disposed between the neighboring first drain wirings, and the second drain wiring has a width of the stripe, which is wider than a minimum width of the stripe of the first drain wiring, "--

and all other limitations as recited in claim 4.

III/ Group III: Claims 7-9:

None of the references of record teaches or suggests the claimed **SEMICONDUCTOR EQUIPMENT** having the limitations:

-- " a plurality of lateral type metal oxide semiconductor transistors having a source cell and a drain cell, which are disposed alternately on a principal plane of the substrate so as to form a mesh pattern; "--

and

-- " the upper layer wiring includes a second source wiring disposed perpendicularly to the first source wiring and having a plurality of stripes for connecting to the first source wiring through a source via-hole, and a second drain wiring disposed perpendicularly to the first drain wiring and having a plurality of stripes for connecting to the first drain wiring through a drain via-hole, wherein the second source wiring has a width of the stripe, which is wider than a minimum width of the stripe of the first source wiring disposed between the neighboring first drain wirings, and the second drain wiring has a width of the stripe, which is wider than a minimum width of the stripe of the first drain wiring, "--

and all other limitations as recited in claim 7.

IV/ Group IV: Claims 16-18:

None of the references of record teaches or suggests the claimed **SEMICONDUCTOR EQUIPMENT** having the limitations:

--" a plurality of transistors having a source cell and a drain cell, "--

and

-- " an upper layer wiring disposed on the lower layer wiring and including a second source wiring for connecting to the first source wiring through a source via-hole and a second drain wiring for connecting to the first drain wiring through a drain via-hole, wherein at least one of the source and drain via-holes has a predetermined pattern so that a length of periphery of the via-hole becomes maximum. "--

and all other limitations as recited in claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Neilson et al. (US patent 5,468,668) disclose a method of forming MOS-gated semiconductor device having mesh geometry pattern.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached at 571-272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thinh T Nguyen TTN

David Nelms
Supervisory Patent Examiner
Technology Center 2800

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